AF
2800

IN THE U.S. PATENT AND TRADEMARK OFFICE

In re Application of:	**Lamson, et al.**	Docket No.:	**TI-28674**
Serial No.:	**09/631,198**	Examiner:	**Nguyen, D.P.**
Filed:	**08/03/2000**	Art Unit:	**2814**
For:	**Structure and Method of High Performance Two Layer Ball Grid Array Substrate**	Conf. No.:	**9326**

11/Appeal Brief
J. Stephan
5-28-03

APPEAL BRIEF TRANSMITTAL FORM

Assistant Commissioner for Patents

Washington, DC 20231

MAILING CERTIFICATE UNDER 37 C.F.R. § 1.8 (A)

I hereby certify that on this day this correspondence is being deposited with the US Postal Service as First Class Mail in an envelope addressed to: Commissioner For Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Elizabeth Austin — Date 5/6/2003

Dear Sir:

Transmitted herewith in triplicate is an Appellant's Brief in the above-identified application.

Charge any additional fees, or credit overpayment to the deposit account of Texas Instruments Incorporated, Account No. 20-0668. An original and two copies of this sheet are enclosed.

Respectfully submitted,

05/27/2003 DSASFAI 00000009 200668 09631198
01 FC:1402 320.00 CH

Michael K. Skrehot
Attorney for Applicant
Registration No. 36,682

Texas Instruments Incorporated
P. O. Box 655474, M.S. 3999
Dallas, Texas 75265
(972) 917-5653

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

	Lamson, et al.	Docket No.:	TI-28674
Serial No.:	09/631,198	Examiner:	Nguyen, D. P.
Filed:	08/03/00	Art Unit:	2814

For: Structure and Method of High Performance Two Layer Ball Grid Array Substrate

Appeal Brief

MAILING CERTIFICATE UNDER 37 C.F.R. §1.8(A)
I hereby certify that this correspondence is being deposited with the U.S. Postal Service as First Class Mail in an envelope addressed to: Commissioner for Patents, PO Box 1450, Alexandria, VA 22313-1450 on
May 6, 2003
Elizabeth Austin

Assistant Commissioner of Patents
Washington, DC 20231

Dear Sir:

Pursuant to the Notice of Appeal mailed 03/06/03, Appellant submits this appeal brief in triplicate. The Commissioner is hereby requested and authorized to charge any fees necessary for the filing of the enclosed papers to deposit account number 20-0668 of Texas Instruments Incorporated.

Real Party in Interest

The real party in interest is Texas Instruments Incorporated.

Related Appeals and Interferences

No related appeals or interferences are known to Appellant.

Status of Claims

Claims 1-22 and 30-36 are pending in this application. Non-elected Claims 23-29 have been cancelled. Claims 1-22 stand allowed. Claims 30-36 are the subject of this appeal.

Claims 30-34 and 36 stand rejected under 35 U.S.C. 102(b) as being anticipated by Stearns, et al. (U.S. Patent No. 6,160,705).

Claim 35 stands rejected under 35 U.S.C. 103(a) as being unpatentable over Stearns in view of Sheldon, et al. (6,259,587).

Status of Amendments

The paper filed by Appellant in response to the final rejection included no amendments. All other amendments have been entered.

Summary of Invention

One embodiment of the invention (see particularly pages 9-12 of the specification) is a packaged integrated circuit including a substrate (110 in Figure 1) having first 113a and second 113b opposing surfaces. The substrate further includes a plurality of signal lines (221 in Figure 2), a plurality of first power lines 222, and a plurality of second power lines 223 on the second surface. One or more of the plurality of signal lines 221 is between a pair of the plurality of first power lines 222. The signal lines between the pair of the plurality of first power lines and the pair of the plurality of first power lines are between a pair of the second power lines 223. (See also Figure 7). The package further includes an integrated circuit chip mounted on the substrate.

Another embodiment of the invention (see also pages 9-12 of the specification) is a packaged integrated circuit including a substrate (110 in Figure 1) having first 113a and second 113b opposing surfaces. The substrate includes a

plurality of lines of at least three different widths on the second surface of the substrate. The lines are arranged such that one or more lines in a first set of lines of a first width (221 in Figure 2) are between lines of the second width (222), and such that one or more lines in a second set of lines of the second width are between lines of the third width (223). (See also Figure 7). The package further includes an integrated circuit chip mounted on said substrate.

Issues

1. Whether Claims 30-34 and 36 are patentable under 35 U.S.C. 102(b) over Stearns, et al. (U.S. Patent No. 6,160,705).

2. Whether Claim 35 is patentable under 35 U.S.C. 103(a) over Stearns in view of Sheldon, et al. (6,259,587).

Grouping of Claims

Claims 30-33 stand or fall together. Claim 34 stands or falls independently of any other claim. Claim 35 stands or falls independently of any other claim.

Argument

1. Claims 30-34 and 36 are patentable under 35 U.S.C. 102(b) over Stearns, et al. (U.S. Patent No. 6,160,705).

Claim 30 includes the feature wherein "one or more of said plurality of signal lines is between a pair of said plurality of first power lines, and further wherein said signal lines between said pair of said plurality of first power lines and said pair of said plurality of first power lines are between a pair of said second power lines." Stearns does not disclose such a feature. Taking the configuration described in the 11/06/02 Office Action with respect to Stearns's Figure 6, for example, signal lines lying between power lines 50 and 56 do not also lie between lines forming Stearns's "enclosed configuration" 58. Enclosed

configuration 58 lies on the opposite side of the substrate layout from the signal lines that lie between power lines 50 and 56. Therefore, Appellant submits that Claim 30 is patentable over Stearns. Claims 31-33 depend on Claim 30 and are therefore patentable over Stearns for at least the reasons presented above.

Claim 34 includes the feature "wherein said lines are arranged such that one or more lines in a first set of lines of a first width are between lines of said second width, and such that one or more lines in a second set of lines of said second width are between lines of said third width." Stearns does not disclose such a feature. The Examiner relies on segments of signal connection features 22 to arrive at the claimed lines of three different widths. Applicant respectfully submits that portions of circular contacts 22 are not lines. A more appropriate comparison would be the straight portions of Stearns's lines, all of the relevant ones of which are the same width. Therefore, Appellant submits that Claim 34 is patentable over Stearns. Claim 36 depends from Claim 34 and is therefore patentable over Stearns for at least the reasons presented above.

2. Claim 35 is patentable under 35 U.S.C. 103(a) over Stearns in view of Sheldon, et al. (6,259,587).

Claim 35 depends from Claim 34 and is therefore distinguished from Stearns for at least the reasons presented above. Sheldon does not cure the deficiencies of Stearns. Since the combined references fail to teach or suggest all of the claimed features of the invention, Appellant respectfully submits that Claim 35 is patentable over Stearns in view of Sheldon. In addition, there is no suggestion in the references for a combination of the teachings of Sheldon with those of Stearns. Stearns's teachings are related to a package and method, whereas Sheldon's teachings are directed to electrical motor safety. The skilled artisan would receive no motivation from either reference for the proposed combination.

Conclusion

In view of the above, Appellant appeals for the reversal of the rejections and allowance of Claims 30-36.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
Phone: 972 917-5653
Fax: 972 917-4418

Michael K. Skrehot
Reg. No. 36,682

APPENDIX

Claims on Appeal

30. A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces, said substrate comprising:

a plurality of signal lines, a plurality of first power lines, and a plurality of second power lines on said second surface, wherein one or more of said plurality of signal lines is between a pair of said plurality of first power lines, and further wherein said signal lines between said pair of said plurality of first power lines and said pair of said plurality of first power lines are between a pair of said second power lines;

an integrated circuit chip mounted on said substrate.

31. The integrated circuit of Claim 30, wherein said signal lines are of a first width, said first power lines are of a second width, and said second power lines are of a third width.

32. The integrated circuit of Claim 31, wherein said third width is wider than said second width, and said second width is wider than said first width.

33. The integrated circuit of Claim 30, further comprising a ground plane on said first surface of said substrate.

34. A packaged integrated circuit, comprising:

a substrate having first and second opposing surfaces, said substrate comprising:

a plurality of lines of at least three different widths on said second surface of said substrate, wherein said lines are arranged such that one or more lines in a first set of lines of a first width are between lines of said second width,

and such that one or more lines in a second set of lines of said second width are between lines of said third width;

an integrated circuit chip mounted on said substrate.

35. The integrated circuit of Claim 34, wherein said lines of said first width are signal lines, said lines of said second width are power lines coupled to a first voltage potential, and said lines of said third width are power lines coupled to a second voltage potential.

36. The integrated circuit of Claim 34, further comprising a ground plane on said first surface of said substrate.